CLAIM:

1. A data processing device comprising
- a register circuit for storing at least two addresses in parallel;
- an address selector arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;
- an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states,
- a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses will be updated as a side-effect of executing the memory access instruction.

2. A data processing device as claimed in claim 1, wherein each control state specifies respective update actions for all of the at least two addresses.

3. A data processing device as claimed in claim 1, wherein the control states comprise states specify a choice from at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value respectively.

4. A data processing device as claimed in claim 1, wherein execution of said memory access instruction causes the execution unit to perform, upon the currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address.

5. A data processing device as claimed in claim 1, the instruction set comprising a load from memory instruction and a store to memory instruction, both causing the instruction execution unit to respond as claimed for said memory access instruction

6. A data processing system comprising a data processing device as claimed in claim 5, programmed with a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively, after setting the control register to one of control states that causes both the first one and the second one of the addresses to be updated.

7. A data processing system comprising a data processing device as claimed in claim 5, programmed with a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively, after setting the control register to one of control states that causes only one of the first or second one of the addresses to be updated.

8. A data processing device as claimed in claim 1, the address selector cycling back and forth between states that select a first and second one of the at least two addresses respectively.

9. A data processing device as claimed in claim 1, the register circuit storing at least three addresses, the address selector cycling through a series of at least three states that select different ones of the at least two addresses.